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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MYERS, PAUL R	
ART UNIT	**PAPER NUMBER**
2112	30

DATE MAILED: 04/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/484,516	HALEPETE ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6,8-39,48-66,76-88 and 93* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8-39,48-66,76-88 and 93* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *22, 23, 27*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 2/13/04 have been fully considered but they are not persuasive.

In regards to applicants argument that "Horden fails to teach or suggest a computer processor determining a frequency and voltage at which to operate a computer processor. Horden may disclose that an operating system determines what frequency and voltage at which to operate a processor": The first part of this argument expressly contradicts the second part. The operating system runs on the processor. Thus the processor determines the frequency and voltage at which to operate the processor. The examiner further notes in accordance with applicants specification the determining is performed by "control software". In Horden the control software is the operating system.

In regards to applicants argument that it would not have been obvious to one of ordinary skill in the art at the time of the invention to modify Horden to arrive at the claimed invention: Since no modification of Horden is required to arrive at the claimed invention this correct.

In regards to applicants argument regarding the "unexpected" advantages between the processor operating system and the processor hardware: Although the claim language does not require the processor determining to be performed without regards to the operating system, i.e. via processor hardware only. The examiner is now citing *Structured Computer Organization* by Tanenbaum. Which teaches the motivations for using hardware or software.

In regards to applicants argument that Claim 16 has been amended to recite that instructions are executed while voltage is changing rather than executing instructions while

voltage is lowering: Horden executes instructions while the voltage is lowered and also while the voltage is changed. Applicants broadening the claim language from lowered to changed does not alleviate the fact the Horden executes instructions while the voltage is lowered which is changing. The examiner believes applicants are trying to argue in accordance with the previous interview that the previous rejection was incorrect in stating that Horden executes instructions while the voltage is lowered. Column 4 lines 32-37 of Horden makes it clear that the operating system causes a change in the voltage in accordance with the application mix currently assessed in the processor core. Both the operating system and the application mix includes instructions that are being executed. Horden in no way states the execution is stopped during the changing of the voltage and frequency and this would have to be expressly stated in Horden to be assumed.

In regards to applicants argument that Horden operating the processor at a number of 6 discrete voltage/frequency pairs: The examiner first does not see the connection between this argument and the claim language. The claim language merely states changing the voltages there is no indication that it is not at discrete voltage/frequencies. Second applicants specification expressly teaches changing the voltage/frequency in a series of small steps which the examiner notes are discrete voltage/frequency pairs. Third Horden teaches supporting a multitude of voltages and frequencies to improve the granularity of power reduction.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 65, 83, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al PN 5,812,860.

In regards to claims 1 and 88: Horden et al teaches a method for controlling the operating condition of a computer processor comprising the steps of: determining a maximum allowable power consumption level from the operating condition of the processor (Column 6 lines 23-25); determining the maximum frequency which provides power not greater than the allowable power consumption level (Column 6 lines 26-30); determining a minimum voltage which allows operation at the maximum frequency determined (Column 6 lines 33-35); and dynamically changing the operating condition of the processor by changing the frequency and voltage to the maximum frequency and minimum voltage determined (Column 6 lines 36-40). Horden et al also teaches the Clock generator, State machine, and Voltage regulator being on a single chip. Horden et al does not expressly teach them being on the same chip as the processor. MPEP 1244.04 V B states making integral is not a patentably distinct. It would have been obvious to a person of ordinary skill in the art to integrate the stare machine/frequency generator in the processor because this would have saved space.

In regards to claim 65: Horden et al teaches calculating the voltage and frequency pairs. Official notice is taken that lookup tables are well known. It would have been obvious to a person of ordinary skill in the art at the time of the invention to maintain the voltage frequency pairs in a lookup table because this would have saved the time in calculating the voltage frequency pairs.

In regards to claims 83: Horden teaches the operating system controlling the voltage and frequencies therefore Horden teaches executing instructions in said computer processor before, during and after changing voltage and frequency.

4. Claims 2-3, 6, 8-11, 78-79 and 87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al PN 5,812,860 in view of Weiss et al PN 5,774,703.

In regards to claims 2, 8, 78-79 and 87: Horden et al teaches a power supply furnishing selectable output voltages (7 and 5); a clock frequency source (8 and 6); a central processor (Figure 1) including: a processing unit (1, 4) for providing values (15) indicative of operating conditions of the central processor; and a clock frequency generator (6) receiving a clock frequency (14) from a clock frequency source (8) and providing a selectable output clock frequency (11) to the processing unit (1, 4); and means for detecting the value indicative of operating conditions of the central processor (6 via 5 and 4) and causing the power supply (7, 5 via 12) and clock frequency generator (6) to furnish an output clock frequency (11) and voltage level (9) for the central processor. Horden et al does not teach the clock generator being able to provide a plurality of frequencies that can be individually selected concurrently. Weiss et al teaches a clock generator for a processor that provides a plurality of clock frequencies which can be individually selected concurrently. It would have been obvious to provide multiple concurrent frequencies because this would have made it easier to optimize different subsystems of the processor (See Weiss abstract). The examiner notes Weiss et al also has the bonus of teaching the clock generator being integrated on the same chip as the rest of the processor (See column 2 where it states figure 1 is a single chip processor).

In regards to claims 3 and 9: Horden et al teaches the means for detecting the values including software (4) for determining the output frequency and power.

In regards to claim 6: Horden et al teaches a power supply furnishing selectable output voltages (7 and 5); a clock frequency source (8 and 6); a central processor (Figure 1) including: a processing unit (1, 4) for providing values (15) indicative of operating conditions of the central processor; and a clock frequency generator (6) receiving a clock frequency (14) from a clock frequency source (8) and providing a selectable output clock frequency (11) to the processing unit (1, 4); and means for detecting the value indicative of operating conditions of the central processor (6 via 5 and 4) and causing the power supply (7, 5 via 12) and clock frequency generator (6) to furnish an output clock frequency (11) and voltage level (9) for the central processor. Horden et al does not teach the clock generator being able to provide a plurality of frequencies that can be individually selected concurrently. Weiss et al teaches a clock generator for a processor that provides a plurality of clock frequencies which can be individually selected concurrently. It would have been obvious to provide multiple concurrent frequencies because this would have made it easier to optimize different subsystems of the processor (See Weiss abstract). The examiner notes Weiss et al also has the bonus of teaching the clock generator being integrated on the same chip as the rest of the processor (See column 2 where it states figure 1 is a single chip processor). Horden teaches the control software being the operating system. Official notice is taken that dedicated software such as firmware is well known. It would have been obvious to use dedicated software as the control program because this would have freed the operating system of these tasks. See also MPEP 2144.04 V C. to make separable.

In regards to claims 10-11: Horden et al teaches adjusting the operating condition of the processor core for optimum operation. Horden et al does not expressly teach the core including a plurality of functional units. Official notice is taken that processor cores with a plurality of functional units is very well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a plurality of functional units in the core because this would have allowed for greater processing capabilities.

5. Claims 13-15, 17-19, 21-23, 26-28, 33-35, 38, 49-51, 53-55, 80-82, and 84-86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al PN 5,812,860 in view of Michail et al PN 5,832,284.

In regards to claims 13-15, 21-23, 33-35, 49-51, 80-82: Horden et al teaches transitioning to higher frequencies and voltages and transitioning to lower frequencies and voltages. Horden et al however does not teach the claimed order of changing clock and voltage. Michail et al teaches when increasing frequency increasing voltage then increasing frequency, and when decreasing frequency decreasing frequency then decreasing voltage (Figure 2). The examiner also notes Michail et al also teaches over-clocking. Michail et al teaches that the reason for the order is stability of the system. It would have been obvious to change the voltages and frequencies in the system in the order of Michail because this would have increased system stability.

In regards to claims 17-19, 26-28, 38, 53-55, 84-86: Horden et al teaches executing instructions before, during and after changing voltage and frequency.

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al PN 5,812,860 in view of Klein PN 5,913,067.

In regards to claim 24: Horden teaches monitoring device utilization which includes data and idle time. Horden also teaches monitoring internal performance data, however Horden et al does not expressly teach that the monitoring of the idle time comprises the monitoring of the internal data. Klein teaches monitoring data transfer to determine device activity to determine device idle time (Column 2 lines 11-23). It would have been obvious to use internal data transfers to determine idle time because this is a standard method of determining idle time especially in consideration of utilization.

7. Claims 30-32, 57-59, and 62-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al PN 5,812,860 in view of Fung et al PN 5,710,929

In regards to claim 30-32, 57-59, 62-64: Horden teaches monitoring processor activity. Horden et al does not teach the activity including a sleep state or a halt state. Fung teaches an activity monitor that handles multiple sleep states including a halt instruction that halts the processor. It would have been obvious to a person of ordinary skill in the art to include multiple sleep states such as Sleep, Doze, and Halt because this would have allowed for multiple user selectable power levels.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 12, 16, 20, 25, 29, 36-37, 39, 48, 56, 60-61, 66, and 76-77 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Horden et al PN 5,812,860.

In regards to claims 12, 48 and 76: Horden et al teaches monitoring operating conditions internal to a computer processor; determining a frequency and a voltage at which to operate said computer processor, based on said internal operating conditions; and implementing the determined frequency and voltage.

In regards to claims 16, 25, 36-37, 39, 52, 72: Horden teaches the operating system controlling the voltage and frequencies therefore Horden teaches executing instructions in said computer processor before, during and after changing voltage and frequency.

In regards to claims 20 and 93: Horden et al teaches monitoring operating conditions including core utilization which includes idle time; determining a frequency and a voltage at which to operate said computer processor, based on said internal operating conditions; and implementing the determined frequency and voltage.

In regards to claims 29, 56 and 61: Horden et al teaches monitoring the state of the processor; determining a frequency and a voltage at which to operate said computer processor, based on said internal operating conditions; and implementing the determined frequency and voltage.

In regards to claim 77: Horden et al teaches a plurality of selectable frequencies.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 3900.

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

PRM
September 4, 2003